Ashwanth Thiyagarajan

(470)-680-8106 | athiyagarajan7@gatech.edu | LinkedIn | GitHub

Summary

Electrical engineering student with hands-on experience in digital design and verification, including SystemVerilog RTL, FSM and datapath development for 32/64-bit processors. Streamlined verification cycles using constrained-random testbenches and assertions, and automated Python scripts to enhance signal clarity by 40%. Skilled in Cadence Xcelium, SimVision and Git, seeking to support logic design efforts for next-generation processor cores.

EDUCATION

Georgia Institute of Technology

Bachelor of Science, Computer Engineering (GPA: 3.78) *Atlanta, GA*

- **Coursework:** Digital Design Laboratory (VHDL/SystemVerilog), Embedded Systems Design, Probability & Statistics for Engineers, Artificial Intelligence for Robotics, Design and Analysis of Algorithms

PROJECTS

Physical Design: RTL-to-GDSII | ***SiliconJackets*** **Mar 2026**

- Orchestrated a complete physical design flow from synthesized netlist to layout using Cadence Genus and Innovus.
- Designed the chip floorplan by structuring sizing, power mesh grids, and manually defining SRAM placements.
- Analyzed LEF files to identify geometric obstruction (OBS) blocks on lower metal layers causing short-circuit.
- Validated physical layouts through parasitic RC extraction (Quantus) and Static Timing Analysis (Tempus).

Design Verification: Class-Based Testbench | ***SiliconJackets*** **Feb 2026**

- Developed driver, monitor, scoreboard, and transaction classes for DUT verification
- Implemented directed and constrained-random stimulus to validate datapath correctness
- Wrote SystemVerilog Assertions (SVA) to verify carry propagation and reset behavior
- Achieved 98% DUT coverage using IMC coverage analysis

DRTL Design: 64-bit Calculator | ***SiliconJackets*** **Feb 2026**

- Designed a synthesizable 64-bit unsigned addition system using modular RTL (32-bit adder chain, result buffer, FSM controller, SRAM interface)
- Implemented multi-cycle FSM sequencing memory reads, carry propagation, and write-back controls
- Ensured synthesizability using alwaysff / alwayscomb and proper non-blocking assignments
- Debugged datapath and control logic using Cadence Xcelium and SimVision waveform analysis

EXPERIENCE

PicklSpot **Jun 2024 - Aug 2024**

Intern – PicklSpot *Alpharetta, GA*

- Developed production software features using SwiftUI and python scripts, delivering functionality that served 1,000+ active users
- Reduced system latency by 30% by profiling the UI with Xcode Instruments and refactoring SwiftUI code, committing changes via Git
- Wrote perl utilities to automate deployment tasks and shell scripts for environment setup, reducing manual steps by 20%

Gravitational Wave Data Analysis (LIGO/Virgo) **Sep 2023 - Jan 2024**

Researcher *Remote*

- Analyzed multi-gigabyte time-series datasets using python and NumPy to identify binary black-hole merger events, applying computer architecture concepts to optimize processing pipelines and enabling the team to prioritize three candidate signals for further study
- Implemented numerical filtering and frequency-domain processing using python and custom perl scripts to improve signal clarity by 40%

Georgia Tech iOS Club **Feb 2026 - Present**

Developer – Georgia Tech iOS Club *Atlanta, GA*

- Collaborate with a team of developers using Xcode and SwiftUI to design and build iOS applications, delivering functional prototypes that enhance club members' learning experience
- Contribute to development of a unified messaging interface that aggregates multi-platform communication streams into a single application
- Follow Git version control and sprint-based Agile cycles to maintain code quality and deliver features on schedule, ensuring reliable releases for club projects

TECHNICAL SKILLS

- **Hardware & Verification:** SystemVerilog (RTL & Testbench), FSM Design, Datapath Design (32/64-bit), Constrained Random Verification, SystemVerilog Assertions (SVA), Coverage Analysis (IMC), Cadence Xcelium, SimVision, Synthesizable RTL-, Memory-Mapped Interfaces, Computer Architecture, Pipelined Designs, Digital Design, Design Verification, Verilog
- **Languages:** C/C++, Python, Java, Swift, Perl, Scripting Languages
- **Frameworks:** SwiftUI
- **Tools:** Linux, Git, Docker, Makefiles, EDA Tools
- **Interests:** Weightlifting, Automotive Engineering, Systems Performance Optimization